REMARKS

Claims 1-10 and 17-21 are pending. Applicant reserves the right to the original and other claims in this and in other applications.

Applicant's representative Ranga Sourirajan had a phone interview with the Examiner on June 4, 2008 and the claims have been amended pursuant to the Examiner's suggestion.

Claims 1, 2, 4-6 and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,821,160 ("Rodriguez"). Applicant respectfully traverses the rejection.

Claim 1 recites a semiconductor apparatus and recites, in part, "an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry; a MOS transistor formed over the semiconductor substrate; and a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array."

Rodriguez is directed to method of manufacturing a random access memory cell using an etch stop layer to form a fuse. (Rodriguez, Abstract; col. 1, lines 6-9). The Office Action contends that Rodriguez teaches all of the limitations of claim 1. (Office Action, pp. 2-5). Applicant respectfully disagrees. Although the Rodriguez device may have a substrate 12, a NMOS transistor and a resistive element 42, it does not disclose "an array of

adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array." Instead, Rodriguez discloses a metal layer 54 which is etched to form "bond pad areas," (Rodriguez, col. 6, lines 48-53) and a polysilicon layer 42 which may be used to form a thin resistor element. (Rodriguez, col. 5, lines 28-29, 34-36). The figures in Rodriguez do not illustrate the "bond pads." The cited portions clearly state that "etch processing is performed to expose bond pads (not illustrated in FIG. 7) . . ." (Rodriguez, col. 6, lines 48-50). Further, Rodriguez does not disclose a bond pad area that is formed such that it extends transversely across an array of adjacent resistive elements. It merely discloses a polysilicon layer 42, which may be used as a resistive element, over nitride spacers 40, and a portion of the metal layer 54 over the polysilicon layer 42. (Rodriguez, FIG. 7; col. 5, lines 25-28).

In contrast, the claimed invention has an electrode pad 31 that extends transversely across an array of adjacent resistive elements 9. (Present Application, Figures 5A-5B) Such a construction, as in the claimed invention, has several advantages over conventional devices. For example, the area of the semiconductor device is reduced and the claimed structure mitigates contamination of the resistive elements by ion impurities, charges, moisture, and thereby stabilizes the resistance values of the resistive elements. (paragraphs [0076]-[0080]). Because Rodriguez does not disclose, teach or suggest all of the limitations of claim 1, Applicant respectfully submits that the 35 U.S.C. §102(b) rejection of independent claim 1 and dependent claims 2 and 4-6 be withdrawn and the claims allowed.

Claim 19 recites a semiconductor apparatus comprising, in part, "an oxide film formed over the semiconductor substrate, the oxide film comprising a resistive-element

formation region, a fuse-element formation region, and a MOS transistor formation region, the resistive-element formation region having a circuit comprising an array of strip-shaped resistive elements formed of a semiconductor material; an insulating layer formed over the oxide film and having an electrode-pad formation region, wherein the electrode-pad formation region is formed over the resistive-element formation region, and wherein the electrode-pad formation region has an electrode pad comprising a metal layer and wherein the electrode pad extends transversely across the array of strip-shaped resistive elements."

As mentioned above, Rodriguez fails to disclose, teach or suggest an electrode pad that extends transversely across an array of strip-shaped resistive elements. Therefore, Applicant respectfully submits that the 35 U.S.C. §102(b) rejection of claim 19 should be withdrawn and the claim allowed.

Claims 1-4 and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,369,409 ("Takasu"). Applicant respectfully traverses the rejection.

Claim 1 recites a semiconductor apparatus and recites, in part, "an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry; a MOS transistor formed over the semiconductor substrate; and a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array."

Takasu is directed to a semiconductor device having a bleeder resistance circuit and a method of making the device. (Takasu, Abstract; col. 1, lines 5-8). The Office Action

contends that Takasu teaches all of the limitations of claim 1. (Office Action, p.5). Applicant respectfully disagrees. Although the Takasu device may have a substrate 801, a N-type transistor and a resistive element 807, it does not disclose "an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry; a MOS transistor formed over the semiconductor substrate; and a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array."

Instead, Takasu discloses an aluminum layer 814 which is deposited by a sputtering method over an intermediate insulating film 812, (Takasu, FIGS. 12E-F, col. 9, lines 38-50) and polysilicon resistors 807. (Takasu, col. 9, lines 28-52). The insulating film 812 having contact holes 813 is deposited over polysilicon resistors 807 and gate electrode 806. (Takasu, FIGS. 12D-F). Takasu does not disclose "bond pads" which are formed over an array of adjacent resistive elements such that the "bond pads" extend transversely across said array of adjacent resistive elements. The Office Action contends that Takasu discloses all of the limitations and that it is *implicit* that part of the aluminum wiring provides contact between an integrated circuit and external circuitry. The cited portions of Takasu only disclose that "although it is not illustrated, the protective film 815 of a region such as a bonding pad is removed." (Takasu, col. 9, lines 54-56). First, the bond pads do not extend transversely across an array of adjacent resistive elements. Second, the Office Action assumes that the aluminum layer 814 comprises an electrode pad. Applicant would like to note that inherency may not be established by probabilities or possibilities.

MPEP § 2112. Because Takasu does not disclose, teach or suggest all of the limitations of claim 1, Applicant respectfully submits that the 35 U.S.C. § 102(b) rejection of independent claim 1 and dependent claims 2-4 and 17 be withdrawn and the claims allowed.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodriguez in view of U.S. Application No. 2002/0063262 ("Matsuzaki"). Applicant respectfully traverses the rejection.

Claim 7 ultimately depends from claim 1 and thus, includes the limitations of claim 1. As such, claim 7 recites, in part, "an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry; a MOS transistor formed over the semiconductor substrate; and a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array."

As mentioned earlier, Rodriguez fails to teach these limitations. Matsuzaki does not cure the above-noted deficiencies of Rodriguez. The Office Action relies on Matsuzaki to teach a rerouting layer formed in a region above the fuse element and an external connection terminal formed on the rerouting layer in a region different from a formation region of the electrode pad. (Office Action, p.8). Because the cited references, individually or in combination, fail to teach or suggest all of the elements of claim 7, Applicant respectfully requests the 35 U.S.C. § 103(a) rejection be withdrawn and claim 7 allowed.

Claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodriguez in view of U.S. Patent No. 6,232,823 ("Tsuchida"). Applicant respectfully traverses the rejection.

Claims 8-10 ultimately depend from claim 1 and thus, include the limitations of claim 1. As such, claims 8-10 recite, in part, "an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry; a MOS transistor formed over the semiconductor substrate; and a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array."

As mentioned earlier, Rodriguez fails to teach these limitations. Tsuchida does not cure the above-noted deficiencies of Rodriguez. The Office Action relies on Tsuchida to teach the additional limitations of claims 8-10. (Office Action, pp.8-10). Because the cited references, individually or in combination, fail to teach or suggest all of the elements of claims 8-10, Applicant respectfully requests the 35 U.S.C. § 103(a) rejection be withdrawn and the claims allowed.

Claims 18 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodriguez in view of U.S. Patent No. 5,107,313 ("Kohda"). Applicant respectfully traverses the rejection.

Claim 18 ultimately depends from claim 1 and thus, includes the limitations of claim 1. As such, claim 18 recites, in part, "an electrode pad comprising a metal layer and formed over the semiconductor substrate, said electrode pad providing contact between said semiconductor apparatus and external circuitry; a MOS transistor formed over the semiconductor substrate; and a circuit formed over said semiconductor substrate and in a region under the electrode pad, said circuit comprising an array of adjacent resistive elements formed of a semiconductor material, said electrode pad being formed over said array of resistive elements such that said electrode pad extends transversely across said array."

As mentioned earlier, Rodriguez fails to teach these limitations. Kohda does not cure the above-noted deficiencies of Rodriguez. The Office Action relies on Kohda to teach gate electrode having lengthwise ends which are bent in an upward direction towards said electrode pad. (Office Action, p.10). Because the cited references, individually or in combination, fail to teach or suggest all of the elements of claim 18, Applicant respectfully requests the 35 U.S.C. § 103(a) rejection be withdrawn and the claim allowed.

Claim 21 ultimately depends from claim 19 and thus, includes the limitations of claim 19. As such, claim 21 recites, in part, "an oxide film formed over the semiconductor substrate, the oxide film comprising a resistive-element formation region, a fuse-element formation region, and a MOS transistor formation region, the resistive-element formation region having a circuit comprising an array of strip-shaped resistive elements formed of a semiconductor material; an insulating layer formed over the oxide film and having an electrode-pad formation region, wherein the electrode-pad formation region is formed over the resistive-element formation region, and wherein the electrode-pad formation

region has an electrode pad comprising a metal layer and wherein the electrode pad extends transversely across the array of strip-shaped resistive elements."

As mentioned earlier, Rodriguez fails to teach these limitations. Kohda does not cure the above-noted deficiencies of Rodriguez. The Office Action relies on Kohda to teach gate electrode having lengthwise ends which are bent in an upward direction towards said electrode pad. (Office Action, p.10). Because the cited references, individually or in combination, fail to teach or suggest all of the elements of claim 21, Applicant respectfully requests the 35 U.S.C. § 103(a) rejection be withdrawn and the claim allowed.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Rodriguez in view of Takasu. Applicant respectfully traverses the rejection.

Claim 20 ultimately depends from claim 19 and thus, includes the limitations of claim 19. As such, claim 20 recites, in part, "an oxide film formed over the semiconductor substrate, the oxide film comprising a resistive-element formation region, a fuse-element formation region, and a MOS transistor formation region, the resistive-element formation region having a circuit comprising an array of strip-shaped resistive elements formed of a semiconductor material; an insulating layer formed over the oxide film and having an electrode-pad formation region, wherein the electrode-pad formation region is formed over the resistive-element formation region, and wherein the electrode-pad formation region has an electrode pad comprising a metal layer and wherein the electrode pad extends transversely across the array of strip-shaped resistive elements."

As mentioned earlier, Rodriguez fails to teach these limitations. Takasu does not cure the above-noted deficiencies of Rodriguez. The Office Action relies on Takasu to

teach low resistance polysilicon region formed immediately next to the lengthwise ends of each resistive element. (Office Action, p.11). Because the cited references, individually or in combination, fail to teach or suggest all of the elements of claim 20, Applicant respectfully requests the 35 U.S.C. § 103(a) rejection be withdrawn and the claim allowed.

A Notice of Allowance is respectfully solicited.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
Ranga Sourirajan
Registration No.: 60,109
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant